TUBF0210 Product Brief

1. Description

The TBUF0210 is a high-performance CMOS Clock Buffer with internal Crystal Oscillator. The XTAL range is from 10MHz to 50MHz, the device has a wide operating voltage from 2.5V to 3.3V. It provides user selectable output VDD option, which provides excellent flexibilities to users. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

2. Applications

- IT infrastructure
- 5G communication
- Automotive electronic

3. Key Features

- 10 single-ended outputs fanout buffer
- Up to 200MHz output frequency
- Ultra-low output additive jitter, the typical value is 50fs
- The input XTAL supports 10MHz to 50MHz, single-ended and differential
- Low output skew, the typical value is 50ps
- User configurable output VDD in different bank:
  - ✧ Mixed 3.3V core，3.3V，2.5V，1.8V or 1.5V output operating supply
  - ✧ Mixed 2.5V core，2.5V，1.8V or 1.5V output operating supply
- Ambient temperature: -40℃~85℃
- Totally Lead-Free & Fully RoHS Compliant
- Halogen and Antimony Free
- Packaged: 5mm×5mm 32-pin QFN

4. Functional Diagram

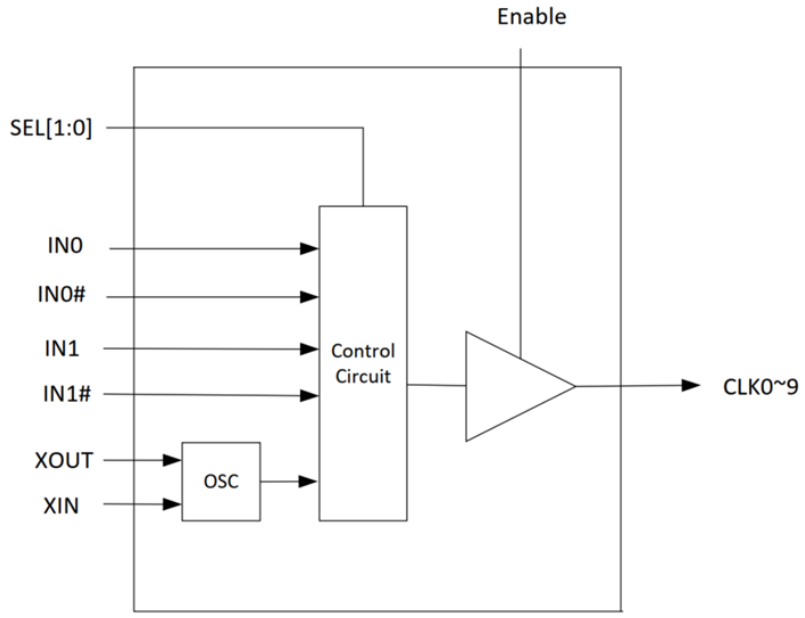

Figure 1 Functional Diagram

5. Pin Maps

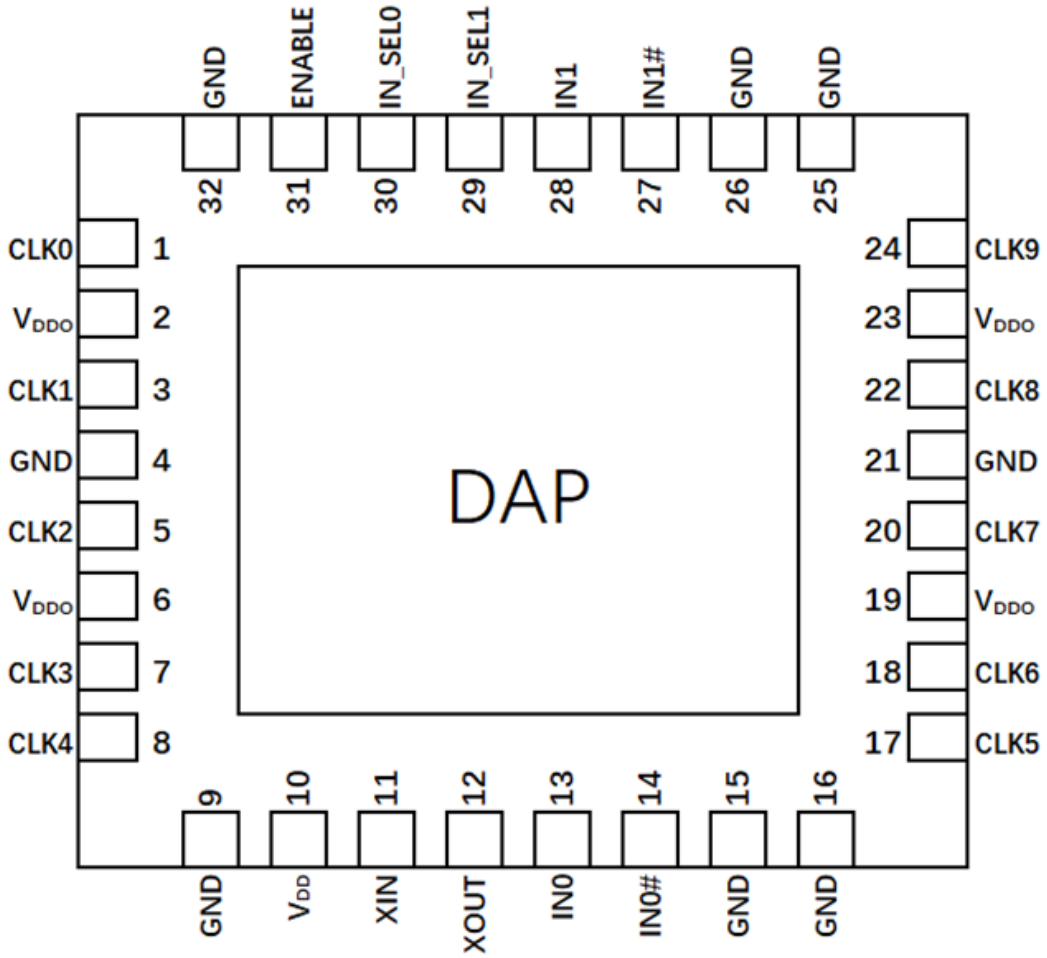

Figure 2 Pin Assignment Diagram-QFN32

6. Pin Descriptions

Table 1 Pin Descriptions

Pin number	Pin name	Type	Description
1	CLK0	Output	Clock Output 0
2	V_{DDO}	Power	Output Supply
3	CLK1	Output	Clock Output 1
4	GND	Power	Ground
5	CLK2	Output	Clock Output 2
6	V_{DDO}	Power	Output Supply
7	CLK3	Output	Clock Output 3
8	CLK4	Output	Clock Output 4
9	GND	Power	Ground
10	V_{DD}	Power	Core Power Supply
11	XIN	Input	Crystal interface
12	XOUT	Output	Crystal interface

13	IN0	Input	REF0 Diff or single-ended
14	IN0#	Input	REF0 Diff，When IN0 is single end ref clock0 and IN0# internal bias as $V_{DD}/2$
15	GND	Power	Ground
16	GND	Power	Ground
17	CLK5	Output	Clock Output 5
18	CLK6	Output	Clock Output 6
19	V_{DDO}	Power	Output Supply
20	CLK7	Output	Clock Output 7
21	GND	Power	Ground
22	CLK8	Output	Clock Output 8
23	V_{DDO}	Power	Output Supply
24	CLK9	Output	Clock Output 9
25	GND	Power	Ground
26	GND	Power	Ground
27	IN1#	Input	REF1 Diff，When IN1 is single end ref clock1 and IN1# internal bias as $V_{DD}/2$
28	IN1	Input	REF1 Diff or single-ended
29	IN_SEL1	Input	Input optional, select XTAL, REF1 and REF0 as input, REF1 and REF0 support Diff or Single End mode
30	IN_SEL0	Input	
31	ENABLE	Input	Active High Output Enable
32	GND	Power	Ground
DAP	DAP	Power	Ground