XAST2104 Product Brief

1. Overview

The XSAT2104 is a four-port, 3 Gbps or 6 Gbps SATA Host Bus Adapter that provides a one-lane PCIe 2.0 interface and SATA controller functions. The XSAT2104 supplies four 6 Gbps SATA ports.

The XSAT2104 supports devices compliant with the Serial ATA International Organization: Serial ATA Revision 3.1 specification. Figure 1 shows the system block diagram.

2. Features

This chapter contains the following information:

- General
- PCIe
- SATA Controller
- SPI Interface Controller
- Peripheral Interface Controller

General

- 1.1V core and 3.3V I/O power supplies.
- Reference clock frequency of 25 MHz, provided by an external clock source or generated by an external crystal oscillator.

PCIe

- PCIe 2.0 endpoint device.
- Compliant with PCIe 2.0 specifications.
- Supports communication speed of 2.5 Gbps and 5 Gbps.
- Supports AHCI programming interface registers for the SATA controller.
- Supports aggressive power management.
- Supports error reporting, recovery and correction.
- Supports Message Signaled Interrupt (MSI).
- Improved PCIe read request efficiency

SATA Controller

- Compliant with Serial ATA Specification 3.1.
- Supports communication speeds of 6 Gbps, 3 Gbps, and 1.5 Gbps.
- Supports programmable transmitter signal levels.
- Supports Gen 1i, Gen 1x, Gen 2i, Gen 2m, Gen 2x, and Gen 3i.
- Supports four SATA ports.
- Supports AHCI 1.0 programming interface.
- Supports Native Command Queuing (NCQ).
- Supports Port Multiplier FIS based switching.
- Supports Partial and Slumber Power Management states.
- Supports Staggered Spin-up.

SPI Interface Controller

- A four-pin interface provides read and write access to an external SPI flash or SPI ROM device.
- Vendor specific information stored in the external device is read by the controller during the chip power-up.
- PCI Boot ROMs of PCIe function 0 can also be stored in the external SPI device and read through the Expansion ROM BAR and the SPI interface controller.

- **Peripheral Interface Controller**
  - ✧ Eight General Purpose I/O (GPIO) ports.
  - ✧ Each of the GPIO pins can be assigned to act as a general input or output pin.
  - ✧ Each of the GPIO inputs can be programmed to generate an edge-sensitive or a level-sensitive maskable interrupt.
  - ✧ Each of the GPIO outputs can be programmed for a connected LED to blink at a user-defined fixed rate. The default rate is 100 ms.

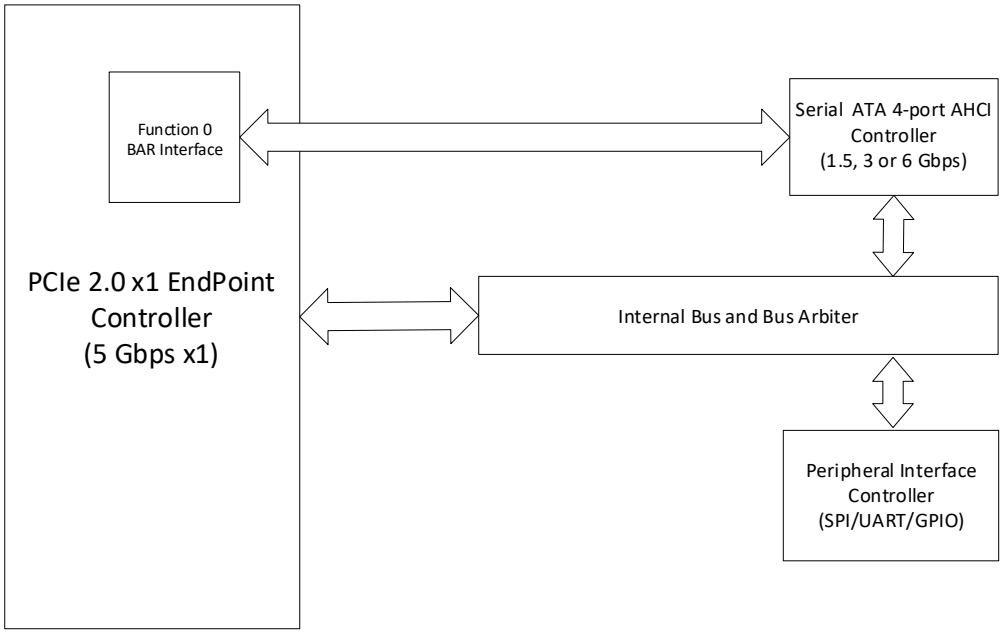

Figure 1 XSAT2104 Architecture(All others)

3. Pin Maps

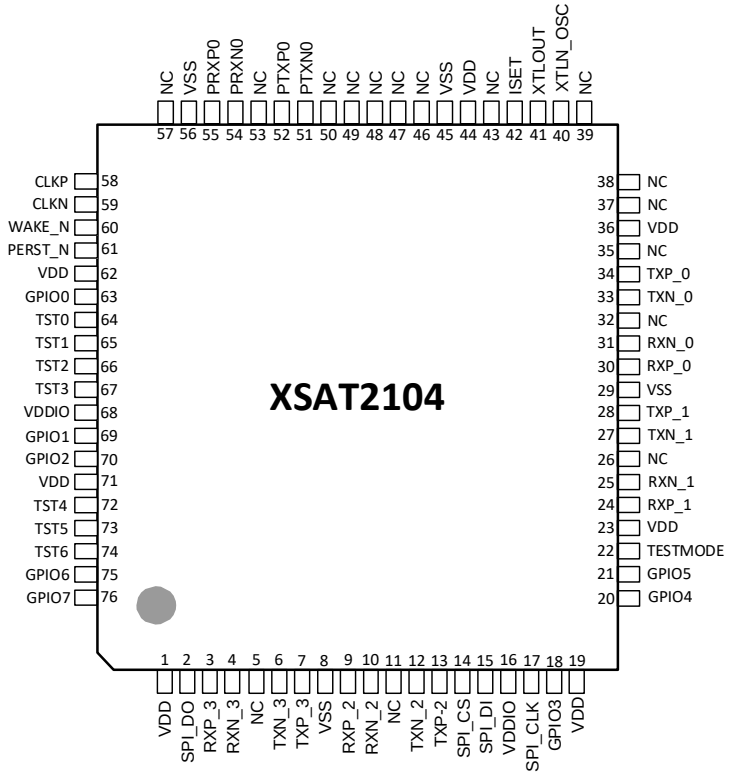

Figure 2 Pin Assignment Diagram

The 76-pin LGA(compatible with QFN), pin diagram is illustrated in Figure 2.

4. Pin Descriptions

Signal Name	Signal Number	Description
PERST_N	61	PCI Platform Reset. Active low, indicates when the applied power is within the specified tolerance and stable.
WAKE_N	60	PCI Wake-Up. An open-drain, active low signal that is driven low by a PCIe function to reactivate the PCIe Link hierarchy's main power rails and reference clocks. **Note:** For applications that support a wake-up function, connect this pin to the WAKE# signal of a PCIe card slot or system board. Connect an external pull-up resistor from the PCIe card slot or system board to the 3.3V auxiliary supply. For applications that do not support a wake-up function, keep the WAKE_N pin on the XSAT2104 open.
CLKP	58	Reference Clock. Low voltage differential signals. The clock frequency has to be 100 MHz.
CLKN	59	
PRXP0	55	PCIe differential signals to the controller's receiver.
PRXN0	54	
PTXP0	52	PCIe differential signals from the controller's transmitter.
PTXN0	51	
TXN_0	33	Serial ATA Transmitter Differential Outputs.
TXP_0	34	
TXN_1	27	
TXP_1	28	
TXN_2	12	
TXP_2	13	
TXN_3	6	
TXP_3	7	
RXN_0	31	Serial ATA Receiver Differential Outputs.
RXP_0	30	
RXN_1	25	
RXP_1	24	
RXN_2	10	
RXP_2	9	
RXN_3	4	
RXP_3	3	
ISET	42	Default is NC If compatible with competitive products, this pin has to be connected to an external 200Ω1% resistor to Ground.
XTLOUT	41	Crystal Output

XTLIN_OSC	40	Reference Clock Input. This signal can be from an oscillator, or connected to a crystal with the XTLOUT pin. The clock frequency must be 25 MHz ± 80 ppm.
GPIO0	63	General Purpose I/O
GPIO1	69	
GPIO2	70	
GPIO3	18	
GPIO4	21	
GPIO5	20	
GPIO6	75	
GPIO7	76	
SPI_CLK	17	SPI Interface Clock.
SPI_DI	15	Serial Data In. Connect to the serial flash device's serial data output (DO).
SPI_CS	14	SPI Interface Chip Select.
SPI_DO	2	Serial Data Out. Connect to the serial flash device's serial data input (DI).
TST0	64	Test Pin 0.
TST1	65	Test Pin 1.
TST2	66	Test Pin 2. This pin is reserved for chip test purposes only. Keep floating.
TST3	67	Test Pin 3. This pin is reserved for chip test purposes only. Keep floating.
TST4	72	Test Pin 4. This pin is reserved for chip test purposes only. Keep floating.
TST5	73	Test Pin 5. This pin is reserved for chip test purposes only. Keep floating.
TST6	74	Test Pin 6. This pin is reserved for chip test purposes only. Keep floating.
TESTMODE	22	Test Mode. Enables chip test modes.
VDDIO	16, 68	I/O Power. 3.3V analog power supply for digital I/Os.
VDD	1, 19, 23, 36, 44, 62, 71	1.1V Core Digital Power.
VSS	8, 29, 45, 56	Ground. The main ground is the exposed die-pad (ePad) on the bottom side of the package.
N/C	35, 37, 43, 46, 47, 49, 50, 57,32,26,11,5,39,53,48,38	No Connect.