1. Description

The XRET5032 is a signal Retimer used to secure the link budget to meet the challenging SI requirements for long PCIe Gen5 channel comprising PCB, connector and cable. It uses advanced signal conditioning techniques to compensate for the channel attenuation and remove the impacts of various jitter sources. It contains 32 Rx-Tx pairs capable of performing up to 32GT/s operation to provide 16-lane Retimer functionalities.

2. Applications

The XRET5032 is targeted for meeting the higher performance PCIe Gen5 interconnection needs of the following end applications:

- Servers
- Storage Appliances
- Hardware Accelerators

3. Key Features

- High Performance Retimer
  - ✧ Compensate for channel loss up to 36dB (die-to-die) by channel comprising PCB, connector and cable
  - ✧ Eliminate deterministic input jitter and random input jitter
  - ✧ Per-lane SerDes configuration (de-emphasis, Rx EQ)
- PCIe Standards and Compatibility
  - ✧ Compliant to PCI Express Gen5 Base Spec.
  - ✧ Support CXL Specification 1.1/2.0
  - ✧ Compliant to Intel PCIe 5.0 Retimer Supplemental Features and Standard BGA Footprint Spec
  - ✧ 32GT/s, 16GT/s, 8GT/s, 5GT/s, and 2.5GT/s Data Rates with Automatic Link Equalization
  - ✧ Compliant to PCIe Gen-5/4/3/2/1
- Clocking
  - ✧ Use standard 100MHz reference clock
  - ✧ Support 100MHz reference clock output
  - ✧ Supports SRIS, SRNS, and Common Clock Systems
  - ✧ Supports upstream and downstream asynchronous clocks
- Power Management
  - ✧ Support the optional L1PM feature of PCI Express
- Support Lane reversal & Lane Polarity Inversion
- Support Hot Plug and Hot Un-Plug
- Support Receive detection bypass
- Automatic identification of port direction
- Support PHY Preset modulation
- Ultra-low latency by architecture optimization(gen5)
  - ✧ Normal Mode : < 36ns
  - ✧ Bypass Mode : < 10ns
- 16 Lanes with Flexible Link Bifurcation Including x2, x4, x8, x16 and each link has an independent PERST#.
- Test and Debug
  - ✧ Support the Rx margining(both Timing and Voltage)Support the slave loop-back
  - ✧ Support eye diagram observe
  - ✧ LTSSM trace
  - ✧ PCIe link EQ logs
  - ✧ Test case generation, detection, and error injection
  - ✧ Real-time error injection
  - ✧ Error count
  - ✧ Observe chip status via pins
  - ✧ Support UART interface, support RS232,

and working baud rate at least 115200bps;

- ✧ Supports the Advanced In-Band Diagnostics

- I2C Interface
  - ✧ Dedicated master interface for external EEPROM configuration loading
- SMBus slave
  - ✧ Dedicated slave interface for configuration programming and debugging registers access
- JTAG Interface
  - ✧ Compliant to IEEE 1149.1/1149.6 AC-JTAG Boundary Scan
- Powered by 0.9V and 1.8V
- 22.8x8.9mm, 354-pin FCCSP, 0.5mm ball spacing package
- RoSH

4. Functional Diagram

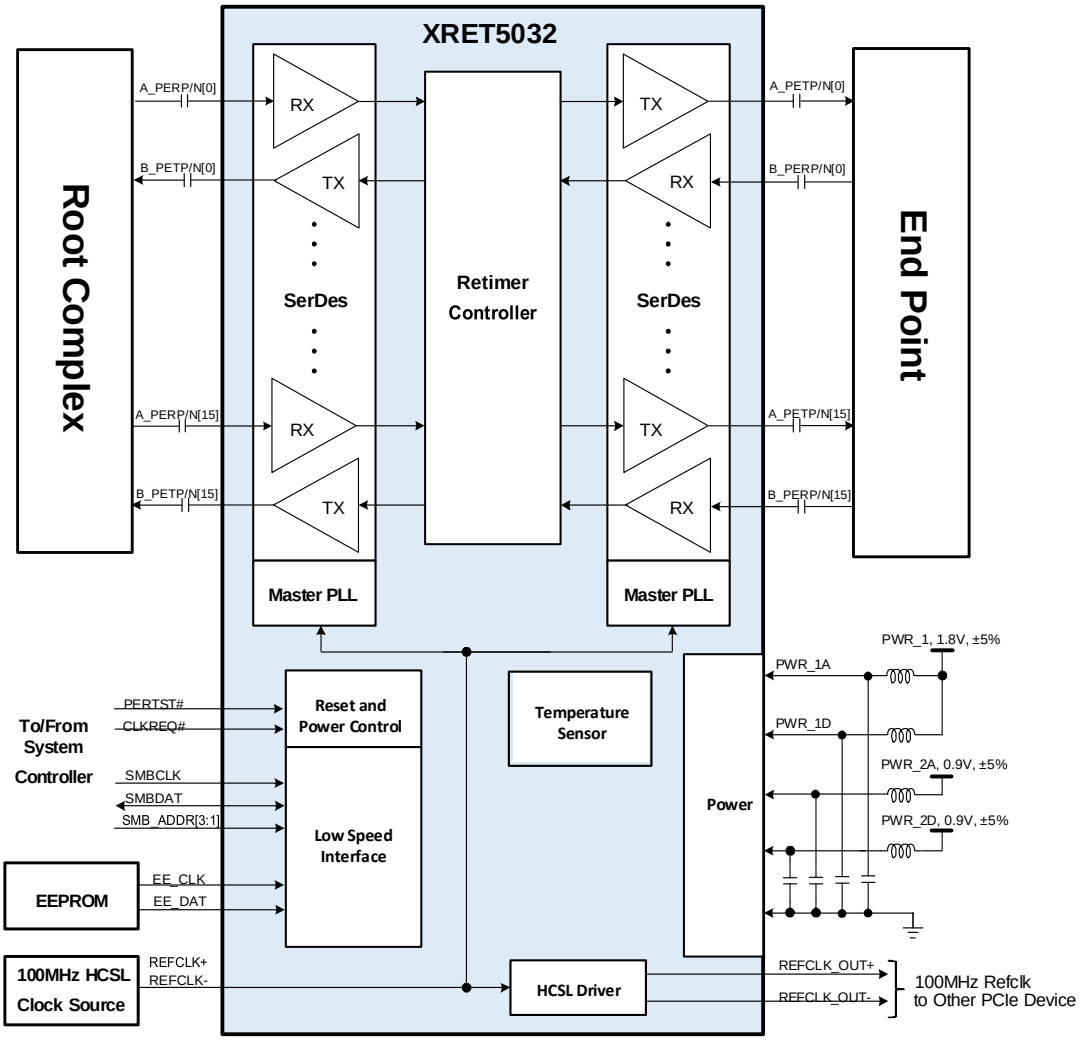

Figure 1 Functional Diagram